Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Title:	**Electronic Circuits I**
Course Number:	**ELE 404**
Semester/Year (e.g.F2016)	**Spring 2024**

Instructor:	**Surinder Jassar**

Report Title	*Design Project*

Submission Date:	Saturday June 22, 2024
Due Date:	Saturday June 22, 2024

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Khan	**Taheer**	**501179194**	**01**	**Taheer Khan**

*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

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Introduction

This document contains the concluding presentation of the ELE 404 Amplifier Design Project. This project assesses a multi-stage amplifier made to satisfy certain requirements, thereby synthesizing the understanding of bipolar junction transistors (BJT) acquired during the course. This project presented an opportunity to put theoretical knowledge to use in a real-world setting and emphasized the value of careful planning, accuracy, and the defense of design choices. The manual calculations for this report can be found attached at the end of the report part of the appendix.

Objectives

The objective of this lab is to design a BJT amplifier with the following requirements:

- Power supply: +10V relative to the ground
- Quiescent current drawn from the power supply: ≤ 10 mA
- No-load voltage gain (at 1 kHz): |Av| = 50 (±10%)
- Maximum no-load output voltage swing (at 1 kHz): ≥ 8 V peak to peak
- Loaded voltage gain (at 1 kHz and with RL = 1 kΩ): ≥ 90% of the no-load voltage gain
- Maximum loaded output voltage swing (at 1 kHz and RL = 1 kΩ): ≥ 4 V peak to peak
- Input resistance (at 1 kHz): ≥ 20 kΩ
- Amplifier type: inverting or non-inverting
- Frequency response: 20 Hz to 50 kHz (−3dB response)
- Type of transistors: BJT
- Number of transistors (stages): ≤ 3
- Resistances permitted: values ≤ 220 kΩ from the E24 series
- Capacitors permitted: 0.1 µF, 1.0 µF, 2.2 µF, 4.7 µF, 10 µF, 47 µF, 100 µF, 220 µF
- Other components (BJTs, diodes, Zener diodes, etc.): only from your ELE404 lab kit

Design Process

To achieve an input resistance of at least 20 kΩ and a desired gain of 50, a three-stage amplifier design was chosen. This design comprises one common cathode (CC) stage and two common emitter (CE) stages. By using the square root of 50, approximately 7.1, the gain calculations were simplified. Setting the gains of the first two stages to -7.1 each brought the total gain close to 50. It was expected that the unity gain of the CC stage would not impact the operating conditions of the first two stages.

Initial Multisim simulations employed DC sweep analysis to create unique graphs. A low collector current of 400 µA was selected for both CE stages, and the same condition was applied to the CC stage due to power supply constraints. These simulations helped determine an operating point, which informed the subsequent manual calculations. Beginning with the final CC stage, the calculation process moved backward to the first stage. The input resistance of the CC stage was calculated and used in the calculations for CE stage 2, ensuring the correct selection of the CC stage's emitter resistor to minimize changes with variations in load

resistance. Using KCL, the value of one resistor was set higher to provide an adequate current divider relative to the base current, determining the values of the biasing resistors.

Since the gains in stages 1 and 2 are identical, stage 1 was calculated in the same manner as stage 2, using the input resistance of the second stage. Thus, the final circuit design included a CC amplifier following two cascading CE stages.

i) Resistors:

The placement of resistors in the circuit required careful consideration of various factors. First, the input resistance of the subsequent stage and the current used were taken into account to calculate the emitter and collector resistors. For example, RE5 = 1 kΩ was selected to minimize significant effects on circuit loading when the load is added or removed.

The emitter degeneration resistors for each stage were chosen based on the intended gain. To find the total required emitter resistance (RE), which is the parallel combination of the emitter resistor and the emitter degeneration resistor, the gain equation was rearranged.

Finally, the remaining biasing resistors were chosen to be as large as possible while still ensuring sufficient current flow. This decision was crucial because very small biasing resistors could significantly reduce the input resistance, causing a notable loading effect on the circuit.

ii) Capacitors:

All capacitors were initially selected based on estimates and later confirmed through calculations. The values were adjusted according to the circuit's operating frequency and the specific positions of each component.

Coupling capacitors C1, C3, and C5, each valued at 10 μF, were placed between amplifier stages. This decision was based on the relatively high input resistances of the stages, meaning significant resistance changes were needed to affect the circuit's overall performance.

Conversely, 100 μF capacitors C2, C4, and C6 were connected to the emitter degeneration resistors. Because small variations in the emitter degeneration resistors could significantly impact the gain, this setup aimed to ensure minimal resistance changes. Thus, using higher capacitance values helped maintain circuit stability despite these variations.

Circuit Under Test

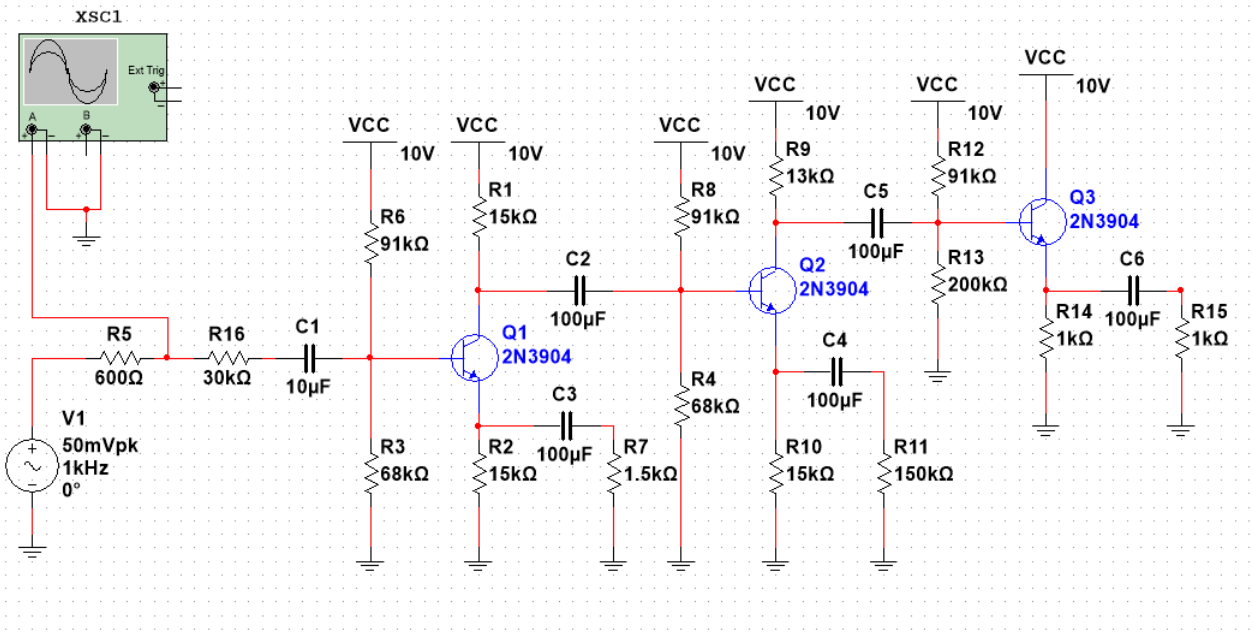


Figure 1: Multisim Circuit Design of 3-stage Amplifier

Experimental Results

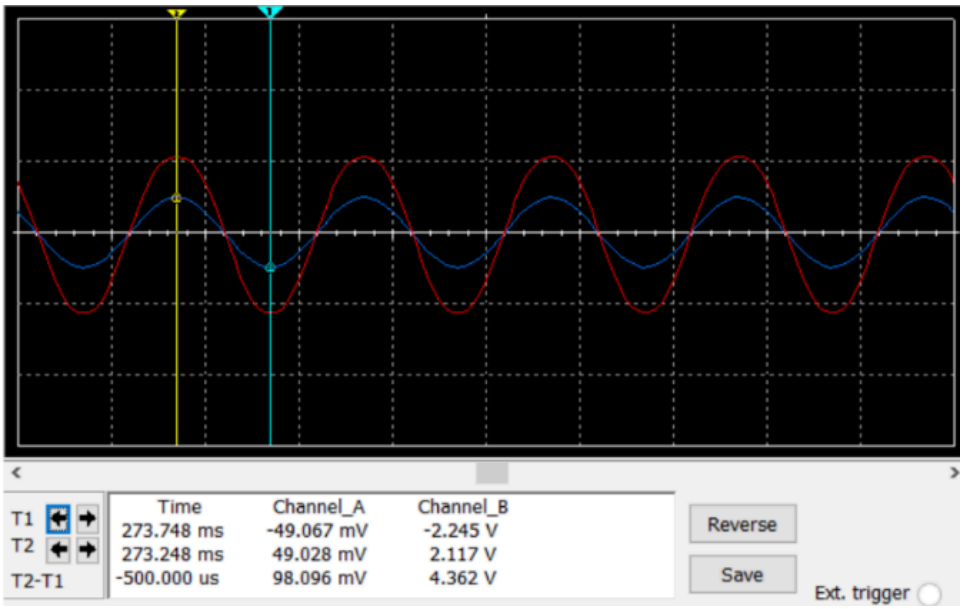


Figure 2: Sinusoidal Waveform for Input and Output Voltages (R_L= 1kΩ)

$V_{I,P-P}$[mV]	$V_{O,P-P}$[mV]	A_{VO}[A/V]
98.1	4.36	44.5

Table 1.0: Input, Output, and Load Voltage Gain for R_L = 1kΩ, frequency = 1kHz

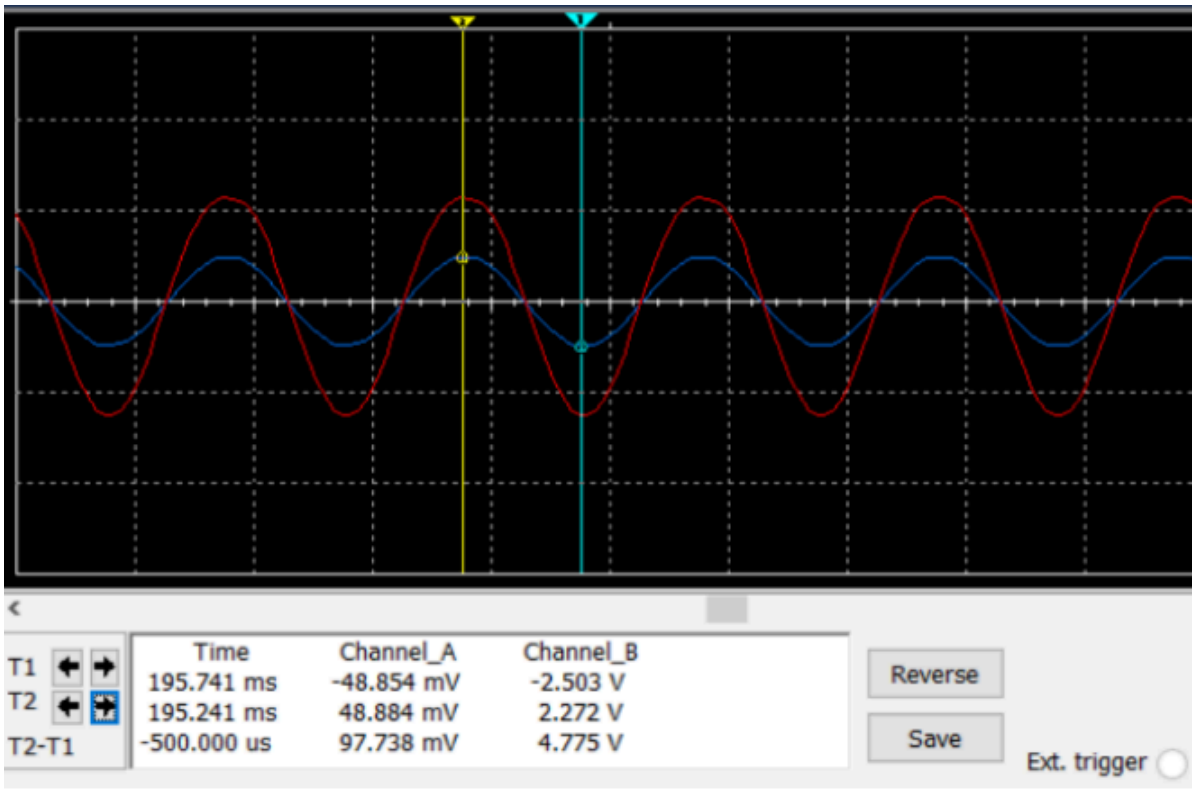


Figure 3: Sinusoidal Waveform for Input and Output Voltages ($R_L = \infty$)

$V_{I,P-P}$[mV]	$V_{O,P-P}$[mV]	A_{VO}[A/V]
97.7	4.78	48.86

Table 2.0: Input, Output, and Load Voltage Gain for $R_L = \infty$, frequency = 1kHz

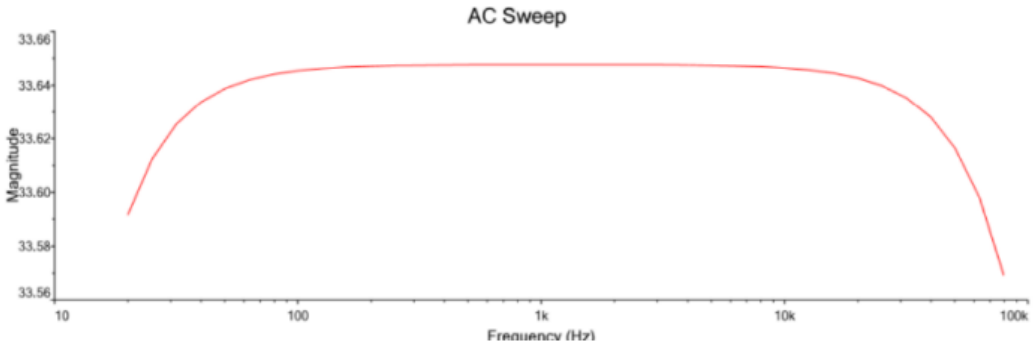


Figure 4: Frequency Response Graph

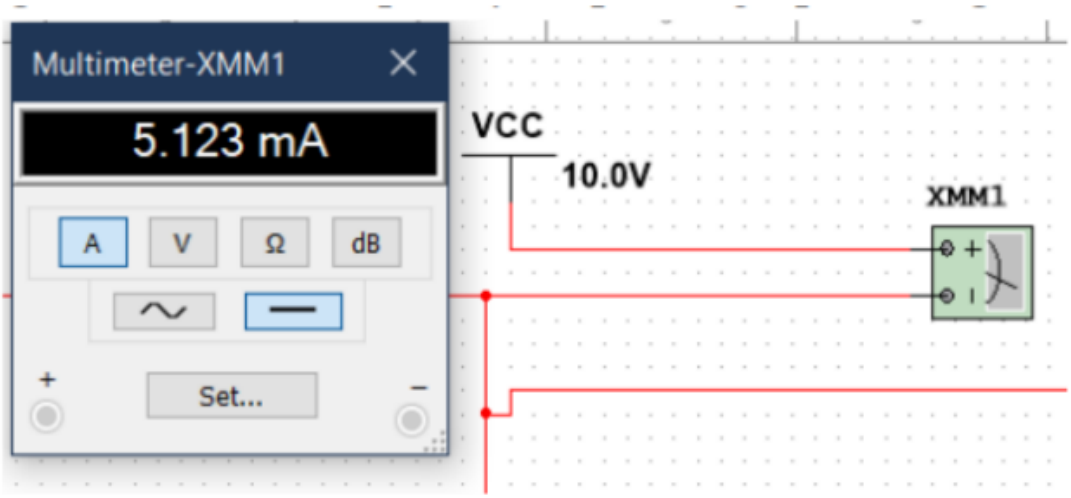


Figure 5: Multimeter Reading for the Quiescent Current

Calculations

R1	R2	R3	R4	R5	R6
91kΩ	68kΩ	91kΩ	68kΩ	91kΩ	200kΩ

Table 3.0: Values for respective Biasing Resistors

C1	C2	C3	C4	C5	C6
10µF	100µF	10µF	100µF	10µF	100µF

Table 4.0: Values for each Capacitor

R_{C1}	R_{C2}	R_{E1}	R_{E2}	R_{E3}	R_{E4}	R_{E5}	R_L
15kΩ	13kΩ	15kΩ	1.5kΩ	15kΩ	1.3kΩ	1kΩ	1kΩ

Table 5.0: Resistor Values for the Collector and Emitter

I_B	$I_{B,DC}$	β	I_C	V	g_m
65mA	30µA	153.8	10mA	5	0.385

Table 6.0: CC Amplifier Values

I_B	$I_{B,DC}$	β	I_C	V	g_m
3.5µA	2µA	114.3	400µA	4.25	0.0154

Table 7.0: CE Amplifier Values

The two characteristic graphs used to draw load lines and initiate the design process are shown below. These graphs plot the collector current flowing through the BJT against the emitter voltage drop.

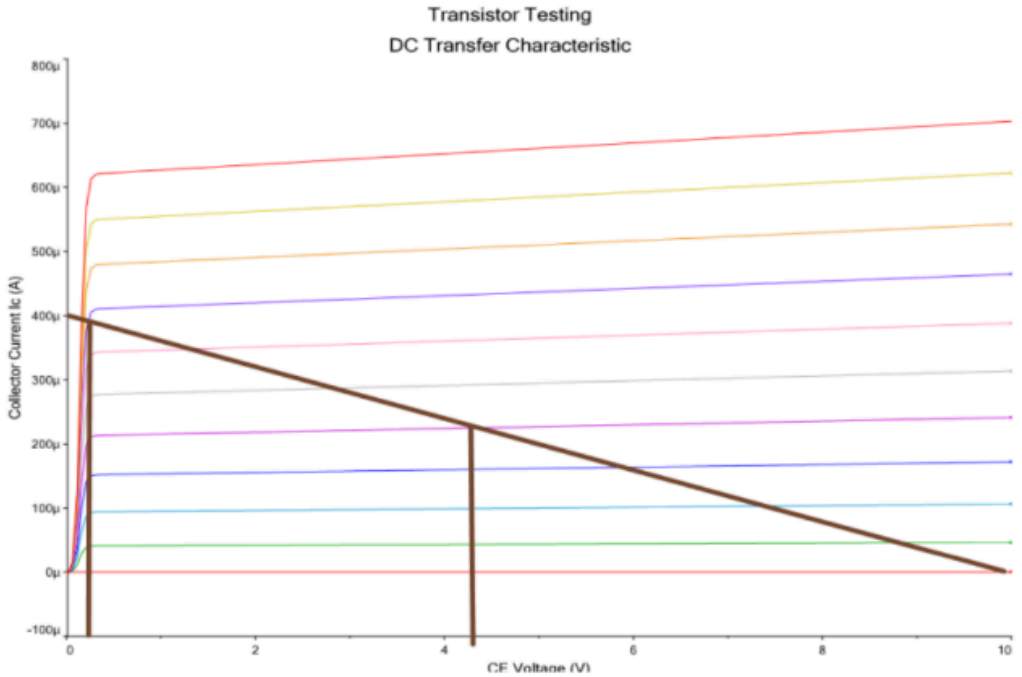


Figure 6: Characteristic graph of CE 2N3904 BJT with load line

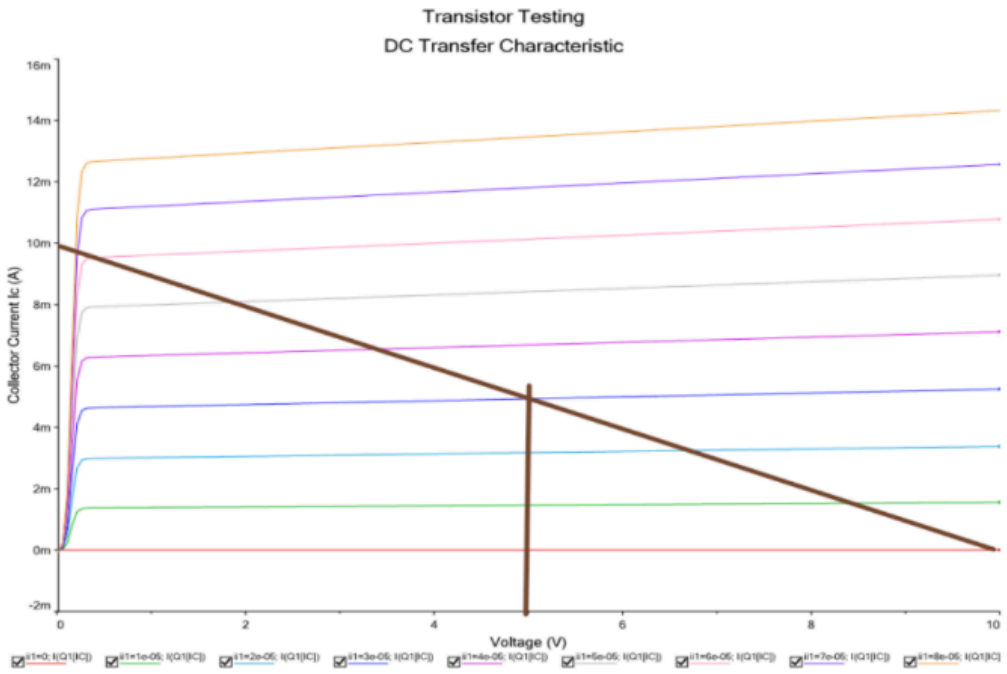


Figure 7: Characteristic graph of CC 2N3904 BJT with load line

Conclusion

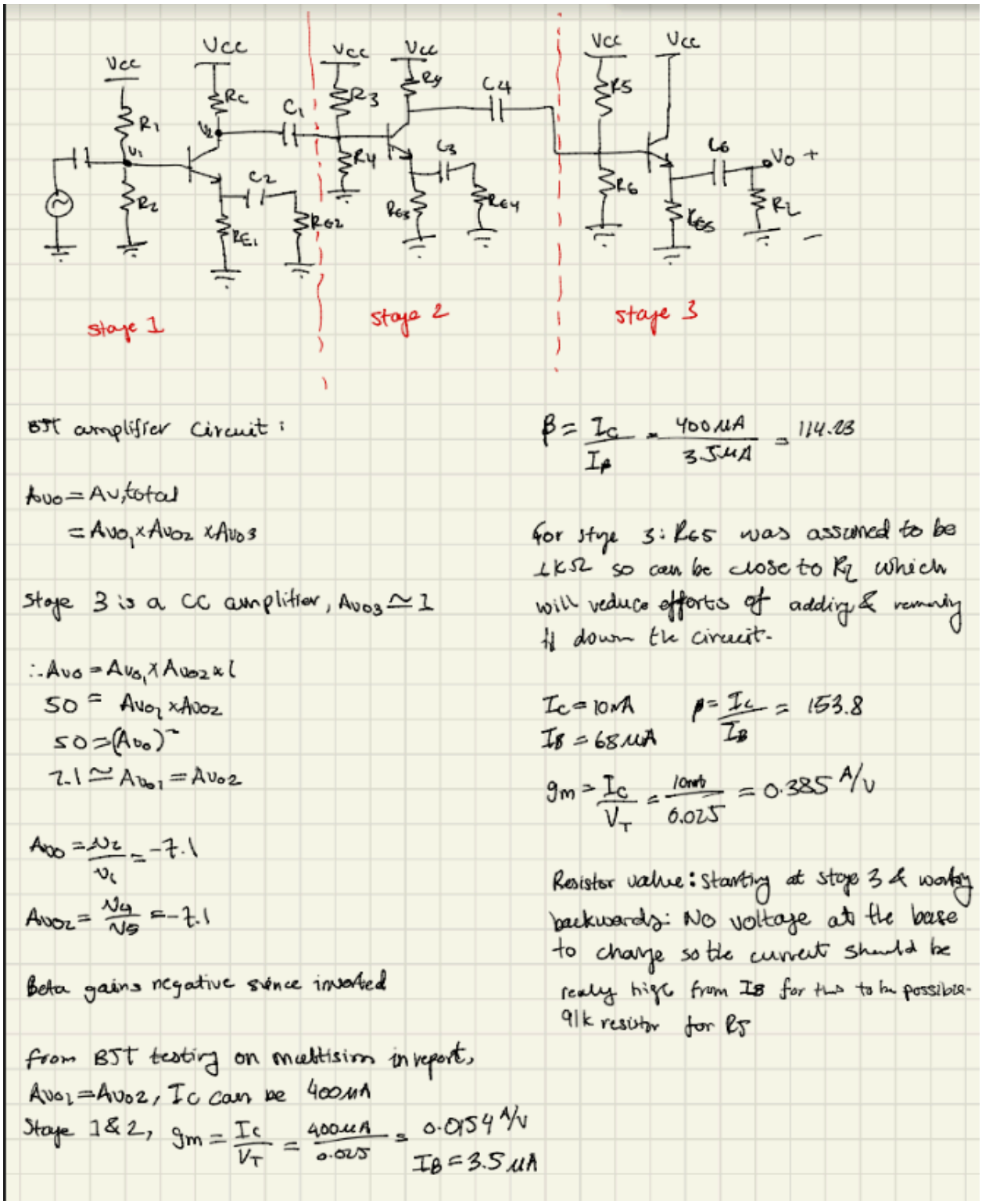
All design criteria were successfully met, with the exception of the no-load voltage swing, which exhibited minor deviations of less than 10%. While hand calculations suggested this possibility, Multisim simulations presented a slight contradiction. This discrepancy might be due to the selection of the operating point from the load line graphs or the biasing approach.

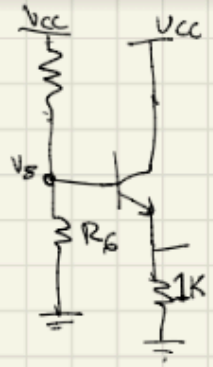
Despite this small variance, all other critical specifications; voltage gain, input resistance, and frequency response were achieved, ensuring no adverse impact on the circuit's performance (see Figure E3). The minor percentage inaccuracies observed in other data likely stemmed from assumptions in the load line graphs and rounding in manual calculations.

In conclusion, the three-stage (CE-CE-CC) configuration effectively met the project's objectives. Both Multisim simulations and manual calculations yielded successful results.

Appendix

Manual calculations attached below:





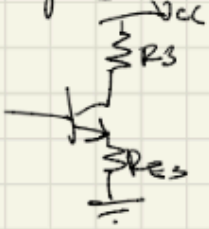
KCL @ V5

$$\frac{5-10}{91k} + \frac{5}{R_6} + 309\mu = 0$$

$$\frac{5}{R_6} - 24.945\mu = 0$$

$$R_6 = 200{,}450\ \Omega$$
$$\simeq 200\ k\Omega$$

Stage 2:



KVL:

$$-4.25 + 0.7 + I_E R_{E3} = 0$$

$$R_{E3} = \frac{3.55}{(1+\beta) I_B} = 15403.97$$

$$R_{E3} \simeq 15k\Omega$$

$$I_{C,DC} = \frac{V_{CC}}{R_C + R_E}$$

$$R_C + R_E = \frac{10^6}{400\mu A} = 25k\Omega$$

$$R_{C,total} = 25k - 15k = 10k\Omega$$

Now, A_v (with load) can be found to check progress

$$R_{in,load} = 91k \,//\, 200k \,//\, \left[\frac{155.8}{0.388} + (154880)\right]$$

$$\Rightarrow 91k\Omega \,//\, 200k\Omega \,//\, 81.3948\Omega$$
$$= 34.67$$

$$R_{in3} = R_3 \,//\, R_{b1} \,//\, \frac{\beta}{g_m} + (\beta+1) R_f$$

$$= 91k \,//\, 200k \,//\, \left[\frac{155.8}{0.585} + 154880\right]$$

$$\simeq 44.57\ k\Omega$$

Since $R_{in3} \,//\, R_{E2}$

$$\frac{1}{R_{total}} = \frac{1}{R_{in3}} + \frac{1}{R_{E2}}$$

$$R_{E2} = 289268\Omega$$

$$\frac{1}{10k} = \frac{1}{44.5k} + \frac{1}{R_{E1}} = 13\Omega$$

$R_{E1\,tot}$ can be found using A_v eqn:

$$A_{v_{E2}} = \frac{-g_m (R_{E2} \,//\, R_{in3})}{1 + g_m R_E}$$

$$R_E = \left[\frac{-0.01545 \cdot (75k \,//\, 44.57k)}{-7.1}\right]$$

$$= 0.0154$$
$$= 1353\Omega$$

$$A_{v2} = \frac{-0.0154\,(134\text{k}\,//\,34.67\text{k})}{1+0.00154\,(135352)}$$

$$\approx -6.663$$

$$\approx -6.7$$

$R_f = 1553 \approx 1.3\text{k} \Rightarrow$ find R_{E4}

Since $R_E = R_{E3}\,//\,R_{E4}$

$$\frac{1}{R_f} = \frac{1}{R_{E3}} + \frac{1}{R_{E4}}$$

$$\frac{1}{R_{E4}} = \frac{1}{\frac{1}{R_E} - \frac{1}{R_{E3}}} = 141836$$

Since no 1.4kΩ in the series using round down to 1.3k. This will cause A_{V2} to increase.

$$I_{C,DC} = \frac{V_{CC}}{R_C+R_{E3}} \to R_C+R_{E3} \cdot \frac{10}{400\mu A}$$

$$R_C+R_{E3} < 25\text{k}\Omega$$

$$R_{E,\text{total}} = 25-15\text{k} = 10\text{k}$$

$R_{E,\text{total}}$: $R_{E1}\,//\,R_{E2}$

$$\frac{1}{10\text{k}} = \frac{1}{R_{E1}} + \frac{1}{31.435\text{k}\Omega}$$

$$R_{E1} = \frac{1}{\frac{1}{10\text{k}} - \frac{1}{31.435\text{k}}} \approx 15\text{k}\Omega$$

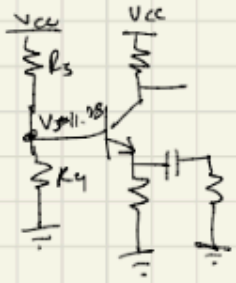
find $R_{F,\text{total}}$:

$$A_{DO_1} = \frac{-g_m\,(R_{E1}\,//\,R_{in2})}{1+g_m R_E}$$

$$R_E = \left[\frac{-g_m\,(R_{E1}\,//\,R_{in2})}{A_{V01}} - 1\right] \div g_m$$

$$= \left[\frac{-0.0154\,(15\text{k}\,//\,31.433\text{k})}{-7.1} - 1\right]$$

Biasing resistors for stage 2:



KVL:

$$\frac{4.25-10}{91\text{k}} + \frac{4.25+2\mu A}{R_4}$$

$$\frac{4.25}{R_4} - 0.000063 = 0$$

$$R_4 = \frac{4.25}{0.000061} = 69459.41$$

$$R_{in} = R_3\,//\,R_4\,//\,\frac{\beta}{g_m} + (\beta+1)R_E$$

$$= 91\text{k}\,//\,68\text{k}\,//\,\frac{114.8}{0.0154} + (115\text{k}\times 155)$$

$$= 31.433\text{k}\Omega$$

$R_4 = 68\text{k}\Omega$

Stage 1: basically a repeat of stage 2

KVL: $-4.25+0.7+I_E R_{E1}=0$

$$-4.25+0.7+(1+\beta)I_B R_E = 0$$

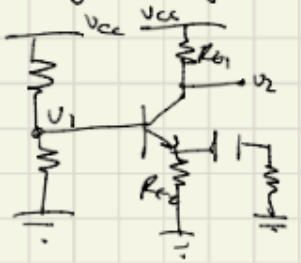
$$R_E = \frac{3.55}{(1+\beta)I_B} = \frac{3.55}{(1+114.25)(2\mu A)} \approx 15\text{k}\Omega$$

$R_{E,\text{total}} = R_{E1}\,//\,R_{E2}$

$$\frac{1}{R_{E\text{total}}} = \frac{1}{R_{E1}} + \frac{1}{R_{E2}}$$

$$R_{E2} = \frac{1}{\frac{1}{R_{E\text{total}}} - \frac{1}{R_{E1}}} \approx 1.5\text{k}\Omega$$

finally assuming $R_1 = 91\text{k}$



$\simeq 1.3K$

KCL @ V_L: $\frac{4.25-10}{91k} + \frac{4.25}{R_2} + 2mA = 0$

$R_2 = 68k\Omega$

Finlly Capacitors

A really low impedance is needed in capacitors, C_1, C_3, C_5 are enclosed to have a low impedance since they already have resistance.

10uf @ lowest for odd numbered capacitors

min 20Hz:

even:

$$Z = \frac{1}{j2\pi(20Hz)(10uF)} = 79.6\Omega$$

odd $Z = \frac{1}{j2\pi(20Hz \times 10uF)}$

$= 79.6\Omega$

middle 1kHz:

$Z = \frac{1}{j2\pi(1000Hz \times 100uF)} = 31.8\Omega$ ← even

odd: $Z = \frac{1}{j2\pi(1000Hz \times 10uF)} = 0.32\Omega$

max: 50Hz

even: $Z \leq \frac{1}{j2\pi(50k \times 100uF)} = 1.6\Omega$

odd: $Z = \frac{1}{j2\pi(50k \times 10uF)} = 15.9\Omega$

Results:

All of the values for the components of the project circuits design were calculated to check total current from each arms

$I_{C_1 DC, total} = I_{C_1} + I_{R_1} + I_{C_2} + I_{R_2} + I_{C_3} + I_{R_3}$

$\Rightarrow \beta I_{B_1} + \frac{V_{CC}}{R_1 + R_2} + \beta I_{B_2} + \frac{V_{CC}}{R_3 + R_4} + \beta I_{B_3} + \frac{V_{CC}}{R_5 + R_6}$

$\Rightarrow \frac{(114 \times 20uA) + 10}{91k + 68k} + \frac{(114.3 \times 20uA) + 10}{91k // 68k}$

$+ 153.8(30uA) + \frac{10}{91k // 200k}$

$\Rightarrow 2.286 \times 10^{-1} uA + 0.06289 mA \times 2] + 4.614 mA + 0.03$

$\Rightarrow 5.23 mA \leq 10 mA$ ✓ passes requirement

Final gain: no load

$A_{V_0} = -7.1 \times 7.1$

$= 50.41$

$A_V = A_{V_1} \times A_{V_2} \times 1$

$= -6.7 \times -7.1$

$= 47.57$

Final Circuit with labelled Values: